

# Low-power single-bit full adder cells

## Cellules d'addition complète 1-bit à faible puissance

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The single-bit full adder is one of the main components in almost all logic structures. The performance of logic structures is highly dependent on the adder cells. This paper discusses the performance of single-bit full adders and presents a performance analysis for those cells in CMOS technology. Fourteen single-bit full adders and three new adders, a total of 17 different adder cells, are analyzed in terms of power and delay using 0.35, 0.25 and 0.18  $\mu\text{m}$  TSMC CMOS technology. In addition, this paper discusses the charging-capability parameter of the adder cells, which represents the fan-out of each cell. The charging-capability parameter is capable of describing the performance of the adder cell in a large, as yet unbuilt structure. Hence, the performance analysis of the single-bit full adder relates the design to power, delay, and charging capability of the logic components.

Un additionneur complet 1-bit est une composante majeure dans presque toutes les structures logiques. Les performances de ces dernières sont liées étroitement à celles des cellules d'addition. Cet article discute des performances des additionneurs complets 1-bit et présente une analyse comparative pour la technologie CMOS. Quatorze additionneurs complets 1-bit et trois nouveaux additionneurs, pour un total de 17 cellules d'addition, sont analysés en termes de puissance et de délai en utilisant les technologies CMOS TSMC de 0.35, 0.25, et 0.18  $\mu\text{m}$ . De plus, l'article étudie le paramètre de capacité de charge des cellules d'addition qui représente la capacité de sortie de chaque cellule. Ce paramètre permet de décrire la performance de la cellule d'addition dans une grande structure potentiellement non construite. Par conséquent, l'analyse de performance de l'additionneur complet 1-bit relie le design à la puissance, le délai et la capacité de charge des composantes logiques.

### I. Introduction

The computationally intensive nature of real-time processing necessitates the use of VLSI implementation. With the rapid advances in VLSI technology, the attributes of parallelism, pipelining, concurrency, and regularity have become a new set of criteria in designing the hardware for digital processing. With highly sophisticated processing schemes at hand and further promising advances in video technology on the horizon, efficient VLSI implementation is of great importance. Broad acceptance of new applications critically depends on the availability of compact and inexpensive hardware delivering the required high performance. Due to the limited power-supply capability of present battery technology, current research efforts face two conflicting design challenges: one is to explore high-performance design and implementation techniques that can meet the stringent speed constraints for real-time systems; the second is to consider low-power design approaches to prolong the operating time of portable devices. To meet these design requirements low-power building blocks with small delay are needed. The power-delay product can be used for first-level comparison between the different building block designs.

The adder is one of the most commonly used building blocks in VLSI design. The full adder cell can be implemented in many different logic structures such as complementary pass-transistor logic (CPL) [1], dual pass-transistor logic (DPL) [2], swing restored pass-transistor logic (SRPL) [3] plus variant (SRPL2) [4], complementary pass-transistor-transmission gate (CPL-TG) [5], or transmission gate logic (TG) plus variant [6]. In this paper, only the static CMOS structure is presented, since it is widely used in parametric design due to its regularity of design.

The performance of the building blocks is one of the main parameters that impact circuit and system performance characteristics. Adder

cells are used to determine the throughput of a processor's executive unit, floating-point unit, and memory address generation [7]. Research has been ongoing to develop low-power adder cells, for low-power digital circuits. Dynamic power dissipation of various adder architectures is compared in [8]. Power-delay characteristics of various adder architectures using static CMOS circuit families are reported in [9]. Using static pass-transistor circuits for low-power applications is suggested in [10]. Various low-power adders have been proposed for low-voltage applications [3]–[5], [11]–[12].

This paper proposes three new single-bit full adder cells and presents a comprehensive study that analyzes the performance of the proposed cells and compares it with that of 14 single-bit full adder cells considered to be the latest currently used CMOS designs for a single-bit full adder cell [13]–[15]. The proposed new full adder cells use a new CMOS XOR-XNOR design [15]. The performance analysis includes power and delay. In addition, this study discusses the charging capability (CC) of the design. The CC parameter defines the limitations of the single-bit full adder cell operation in a larger logic structure without requiring the structure to be built. A multi-bit adder can present the larger logic structure. The performance analysis was done using 0.35, 0.25, and 0.18  $\mu\text{m}$  TSMC technology.

The rest of this paper is organized as follows: Section II reviews the latest designs of single-bit full adder cells; Section III introduces the proposed single-bit full adder cells; Section IV describes the large logic structure (i.e., multi-bit adder) and briefly explains the different multi-bit adder methods of design; Section V discusses power and delay parameters for VLSI logic circuits; Section VI illustrates the experimental setup; Section VII discusses the performance analysis and the results; Section VIII shows the requirements of the charging-capability parameter; and Section IX concludes the paper.

### II. Single-bit full adder structures

CMOS technology has been improving over the past century to the extent that IC layout designers are now using 0.13  $\mu\text{m}$  technology. Fur-

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